Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **14EC2071** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VLSI SUBSYSTEM DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Explain the CMOS system design based on the data path operators with a suitable example. | CO1 | 10 |
| b. | Draw and explain the basic memory chip architecture. | CO1 | 10 |
| (OR) | | | | |
| 2. | a. | Design a logic for an ALU that performs these functions: 1) a AND b, 2) a OR b, 3) a XOR b, 4) NOT a, 5) a + b, 6) a -b. | CO1 | 10 |
| b. | Draw a transistor-level circuit diagram for a 6T- SRAM core cell and explain the working principle in read, write and current sensing circuit. | CO2 | 10 |
|  |  |  |  |  |
| 3. | a. | Design the logic 4\*4 structure of Ripple Carry adder and explain its working principle. | CO2 | 15 |
| b. | Sketch the Flow diagram of Serial/Parallel multiplier. | CO1 | 5 |
| (OR) | | | | |
| 4. | a. | Sketch the structure of binary subtraction and explain its working principle for the function A-B. | CO2 | 15 |
| b. | Recall the Flow diagram of Wallace tree multiplier. | CO1 | 5 |
|  |  |  |  |  |
| 5. |  | Design 16 bit Synchronous counter using J-K FF with its timing diagram. | CO3 | 20 |
| (OR) | | | | |
| 6. | a. | Design 3 bit Asynchronous counter using T FF with its timing diagram. | CO3 | 15 |
| b. | Classify the different Clocking Strategies with its block and timing diagram. | CO3 | 5 |
|  |  |  |  |  |
| 7. | a. | Design the logic 5\*6 structure of Wallace-tree multiplier and explain its working. | CO2 | 10 |
| b. | Discuss on Funnel shifters with an example. | CO2 | 10 |
| (OR) | | | | |
| 8. | a. | Explain the functionality of CAM operation with its structure. | CO2 | 12 |
| b. | Give a complete table of the barrel shifters possible operation. List all the possible combinations of top and bottom input, and the resulting operation. | CO2 | 8 |
|  | |  |  |  |
|  | | **Compulsory**: |  |  |
| 9. |  | Considering the following Boolean function and design a combinational circuit using PLA and PAL. The designed function should exhibit in a single structure. | CO2 | 20 |